CLAIMS

1. An unpredictable microprocessor or microcomputer comprising a processor (1), a first working memory (51), a main memory (6) containing an operating system a main program (P1) and a secondary program (P2), characterized in that it also has:

- a second working memory (52);

- switching means that make it possible, while the programs are running, to switch from using one of its two working memories (51, 52) to using the other working memory, while saving their contents;

- these switching means comprising at least one block of registers (54) for storing the operating context of the programs in the main memory, and a switching circuit (53) for enabling one of the working memories and the access registers (A1-A3)(D1-D3) associated with each memory (51, 52, 6) and controlled by said switching circuit (53).

2. The unpredictable microprocessor or microcomputer according to claim 1, characterized in that it has a second block of registers (55) for storing the operating context of the secondary program.

3. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that it has means (R1, R2, R3) for de-correlating the running of the programs from an isochronous clock.

4. The microprocessor or microcomputer according to any of the preceding claims, characterized in that the main programs can enable or inhibit the switching mechanism or mechanisms by loading the circuit (53) for switching and enabling the working memories (51, 52) and the blocks of storage registers (54, 55) associated with each respective working memory (51, 52).

5. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that the second working memory (52) and its access registers (A3, D3) are substituted for the working memory (51) and its access registers (A2, D2) in its utilization by a main program.

6. The unpredictable microprocessor or microcomputer according to claim 3, characterized in that the de-correlating means comprise a random number generator (2) that makes it possible to trigger, via the interrupt circuit (4) a random interrupt for desynchronizing

the running of the programs in the processor, by randomly jumping to the secondary program (P2).

7. The microprocessor or microcomputer according to claim 4 or 6, characterized in that the de-correlating means comprise a time counting system (R3) independent from the processor (1) that makes it possible, after the time count, to trigger an interrupt for returning from the secondary program to the main program.

8. The unpredictable microprocessor or microcomputer according to claim 4, 6 or 7 or a combination thereof, characterized in that the means (53, 54, 55, A2, A3, D2, D3) for switching working memories is controlled by the processor and its program, by the random interrupt system (2, 4), by a timer (R3), or by any combination of at least two of the three.

9. The unpredictable microprocessor or microcomputer according to any of the preceding claims or a combination thereof, characterized in that the means (53, 54, 55, A2, A3, D2, D3) for switching working memories is enabled by being loaded by the processor (1) running a main program sequence.

10. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that the secondary program (P2) uses a working space identical to that of the main program (P1) in the main memory (6).

11. The unpredictable microprocessor or microcomputer according to any of claims 1 through 9, characterized in that the secondary program (P2) uses a working space smaller than that of the main program.

12. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that the switching means carry out the substitution of the memories (51, 52, 53, 54, 55, A2, A3, D2, D3) and the associated contexts within the execution cycle of an instruction from the microprocessor.

13. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that the secondary program (P2) does not modify the general operating context of the main program (P1) in order to allow the latter to return without having to reestablish this context.

14. The unpredictable microprocessor or microcomputer according to claim 13, characterized in that the context of the main program (P1) is reestablished either automatically by the secondary program (P2) or automatically by the switching means (53) before returning control to the main program (P1).

15. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that it comprises means for substituting the memory of the secondary program (P2) for the memory of the main program (P1).

16. The unpredictable microprocessor or microcomputer according to any of the preceding claims, characterized in that the main program (P1) can use the first working memory (51) and/or the second working memory (52) alternately or simultaneously.

17. The unpredictable microprocessor or microcomputer characterized in that the loading of the switching circuit (53) makes it possible to mask or unmask the de-correlating interrupts.

18. The unpredictable microprocessor or microcomputer, characterized in that the return to the main program (P1) is carried out by an interrupt triggered by the secondary

program (P2) after the switching register (53) has been properly loaded, by executing an instruction of the main program (P1) or the secondary program (2), in order to unmask the interrupts.

1. 19. The unpredictable microprocessor or microcomputer, characterized in that it is embodied in a monolithic integrated circuit.

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